

## Different Groups of Instructions in Instruction Set of 8088/8086:

### Instruction Set:-

- The instruction set of a microprocessor defines the basic operations that a programmer can make the device perform.
- The instruction set of 8088/8086 microprocessor has 117 basic instructions.

	<u>CMPSB</u>	<u>JAE</u>	<u>JNBE</u>	<u>JPO</u>	<u>MOV</u>	<u>RCR</u>	<u>SCASB</u>
<u>AAA</u>	<u>CMPSW</u>	<u>JB</u>	<u>JNC</u>	<u>JS</u>	<u>MOVSB</u>	<u>REP</u>	<u>SCASW</u>
<u>AAD</u>	<u>CWD</u>	<u>JBE</u>	<u>JNE</u>	<u>JZ</u>	<u>MUL</u>	<u>REPE</u>	<u>SHL</u>
<u>AAM</u>	<u>DAA</u>	<u>JC</u>	<u>JNG</u>	<u>LAHF</u>	<u>NEG</u>	<u>REPNE</u>	<u>SHR</u>
<u>AAS</u>	<u>DAS</u>	<u>JCXZ</u>	<u>JNGE</u>	<u>LDS</u>	<u>NOP</u>	<u>REPNZ</u>	<u>STC</u>
<u>ADC</u>	<u>DEC</u>	<u>JE</u>	<u>JNL</u>	<u>LEA</u>	<u>NOT</u>	<u>REPZ</u>	<u>STD</u>
<u>ADD</u>	<u>DIV</u>	<u>JE</u>	<u>JNLE</u>	<u>LES</u>	<u>OR</u>	<u>RET</u>	<u>STI</u>
<u>AND</u>	<u>HLT</u>	<u>JG</u>	<u>JNO</u>	<u>LODSB</u>	<u>OUT</u>	<u>RETF</u>	<u>STOSB</u>
<u>CALL</u>	<u>IDIV</u>	<u>JGE</u>	<u>JNP</u>	<u>LODSW</u>	<u>POP</u>	<u>ROL</u>	<u>STOSW</u>
<u>CBW</u>	<u>IMUL</u>	<u>JL</u>	<u>JNS</u>	<u>LOOP</u>	<u>POPA</u>	<u>ROR</u>	<u>SUB</u>
<u>CLC</u>	<u>IN</u>	<u>JLE</u>	<u>JNZ</u>	<u>LOOPE</u>	<u>POPF</u>	<u>SAHF</u>	<u>TEST</u>
<u>CLD</u>	<u>INC</u>	<u>JMP</u>	<u>JNZ</u>	<u>LOOPNE</u>	<u>PUSH</u>	<u>SAL</u>	<u>XCHG</u>
<u>CLI</u>	<u>INT</u>	<u>JNA</u>	<u>JO</u>	<u>LOOPNZ</u>	<u>PUSHA</u>	<u>SAR</u>	<u>XLATB</u>
<u>CMC</u>	<u>INTO</u>	<u>JNAE</u>	<u>JP</u>	<u>LOOPZ</u>	<u>PUSHFD</u>	<u>SBB</u>	<u>XOR</u>
<u>CMP</u>	<u>IRET</u>	<u>JNB</u>	<u>JPE</u>		<u>RCL</u>		
		<u>JA</u>					

- The wide range of operands and addressing modes permitted for use with these instructions executable at the machine code level.

- The instruction set can be divided into a number of groups of functionally related instructions.

1. Data Transfer Instructions.
2. Arithmetic Instructions.
3. Compare Instructions.
4. Logic Instructions.
5. Shift Instructions.
6. Flag control Instructions.
7. Stack operations Instructions.
8. Jump Instructions.
9. Rotate Instructions.
10. Subroutine handling Instructions.
11. String handling Instructions.

2. Isolated I/O Instructions.
4. Logic Instructions.
6. Shift Instructions.
8. Flag control Instructions.
10. Subroutine handling Instructions.
12. Loop handling Instructions.

### DATA TRANSFER INSTRUCTIONS

GENERAL-PURPOSE BYTE OR WORD TRANSFER INSTRUCTIONS	SIMPLE INPUT AND OUTPUT PORT TRANSFER INSTRUCTION	SPECIAL ADDRESS TRANSFER INSTRUCTION	FLAG TRANSFER INSTRUCTIONS
MOV PUSH POP XCHG XLAT/XLATB	IN OUT	LEA LDS LES	LAHF SAHF PUSHF POPF

### ARITHMETIC INSTRUCTIONS

ADDITION INSTRUCTIONS	SUBTRACTION INSTRUCTIONS	MULTIPLICATION INSTRUCTIONS	DIVISION INSTRUCTIONS
ADD	SUB	MUL	DIV
ADC	SBB	IMUL	IDIV
INC	DEC	AAM	AAD
AAA	NEG		CBW
DAA	CMP		CWD
	AAS		
	DAS		

### BIT MANIPULATION INSTRUCTIONS

LOGICAL INSTRUCTIONS	SHIFT INSTRUCTIONS	ROTATE INSTRUCTIONS
NOT AND OR XOR TEST	SHL / SAL SHR SAR	ROL ROR RCL RCR

## STRING INSTRUCTIONS

<b>STRING INSTRUCTIONS</b>	
REP	
REPNE / REPZ	
REPNE / REPNZ	
MOVS / MOVS B / MOVS W	
COMPS / COMPS B / COMPS W	
SCAS / SCAS B / SCAS W	
LODS / LODSB / LODSW	
STOS / STOSB / STOSW	

## PROGRAM EXECUTION TRANSFER INSTRUCTIONS

<b>UNCONDITIONAL TRANSFER INSTRUCTIONS</b>	<b>CONDITIONAL TRANSFER INSTRUCTIONS</b>	<b>ITERATION CONTROL INSTRUCTIONS</b>	<b>INTERRUPT INSTRUCTIONS</b>	
CALL RET JMP	JA / JNBE JAE / JNB JB / JNAE JBE / JNA JC JE / JZ JG / JNLE JGE / JNL JL / JNGE	JLE / JNG JNC JNE / JNZ JNO JNP / JPO JNS JO JP / JPE JS	LOOP LOOPE / LOOPZ LOOPNE / LOOPNZ JCXZ	INT INTO IRET

## PROCESS CONTROL INSTRUCTIONS

<b>FLAG SET/CLEAR INSTRUCTIONS</b>	<b>EXTERNAL HARDWARE SYNCHRONIZATION INSTRUCTIONS</b>
STC CLC CMC STD CLD STI CLI	HLT WAIT ESC LOCK NOP

**Note:**

Here, I explain them under:

**2-operand instructions**

Ex. ADD BX, CX

**1-operand instructions**

Ex. PUSH SI

**0-operand instructions:**

Ex. DAA

## **Data Transfer Instructions: -**

- These instructions are used to transfer data from source to destination.
- The operand can be a constant, memory location, register or I/O port address.
- \* Move byte or word (MOV) Instruction.
- \* Exchange byte or word (XCHG) Instruction.
- \* Translate byte (XLAT) Instruction.
- \* Load effective address (LEA) Instruction.
- \* Load data segment (LDS) Instruction.
- \* Load extra segment (LES) Instruction.

**Note:** We are going to investigate these instructions in details

Mnemonic	Function
MOV	Move byte or word to register or memory
IN, OUT	Input byte or word from port, <u>output</u> word to port
LEA	Load effective address
LDS, LES	Load pointer using data segment, extra segment
PUSH, POP	Push word onto stack, pop word off stack
XCHG	Exchange byte or word
XLAT	Translate byte using look-up table

## MOV Instruction

- MOV instruction is used to transfer a byte or a word of data from a source operand to a destination operand.
- It does not modify flags.

Mnemonic	Meaning	Format	Operation	Flags affected
Mov	Move	Mov D,S	(s) → (D)	None

MOV	
Memory	Accumulator
Accumulator	Memory
Register	Register
Register	Memory
Memory	Register
Register	Immediate
Memory	Immediate
Seg reg	Reg 16
Seg reg	Mem 16
Reg 16	Seg reg
Mem	Seg reg

## NO MOV

Mem → Mem  
 Imm → Seg Reg  
 Seg Reg → Seg reg

MOV reg8, r/m/i8  
 MOV mem8, reg8  
 MOV mem8, BYTE imm8

MOV reg16, r/m/i16  
 MOV mem16, reg16  
 MOV mem16, WORD imm16

MOV r/m16, segreg  
 MOV segreg, r/m16

## MOV d,s

d=destination (register or effective memory address),  
s=source (immediate data, register or memory address)

MOV can transfer data from:

- any register to any register (except CS register)
- memory to any register (except CS)
- immediate operand to any register (except CS)
- any register to a memory location
- immediate operand to memory
- MOV cannot perform memory to memory transfers (must use a register as an intermediate storage).
- MOV moves a word or byte depending on the operand bit-lengths; the source and destination operands must have the same bit length.
- MOV cannot be used to transfer data directly into the CS register.
- The number of clock cycles needed for an instruction depends on the addressing mode.
- For 8088/8086 systems, calculation of the effective address (16 bits) of the operand can take several clock cycles (these extra clock cycles are not needed for 80286 or later microprocessors):

Examples Extra clock cycles needed for calculating effective address:

Addressing mode	Example	Clock
register indirect	MOV CL,[DI]	5
Direct	MOV CL,FRED	3
Based index	MOV BL,[BP+DI]	7
Based index (displacement)	MOV CX,[BP+DI+FRED]	11

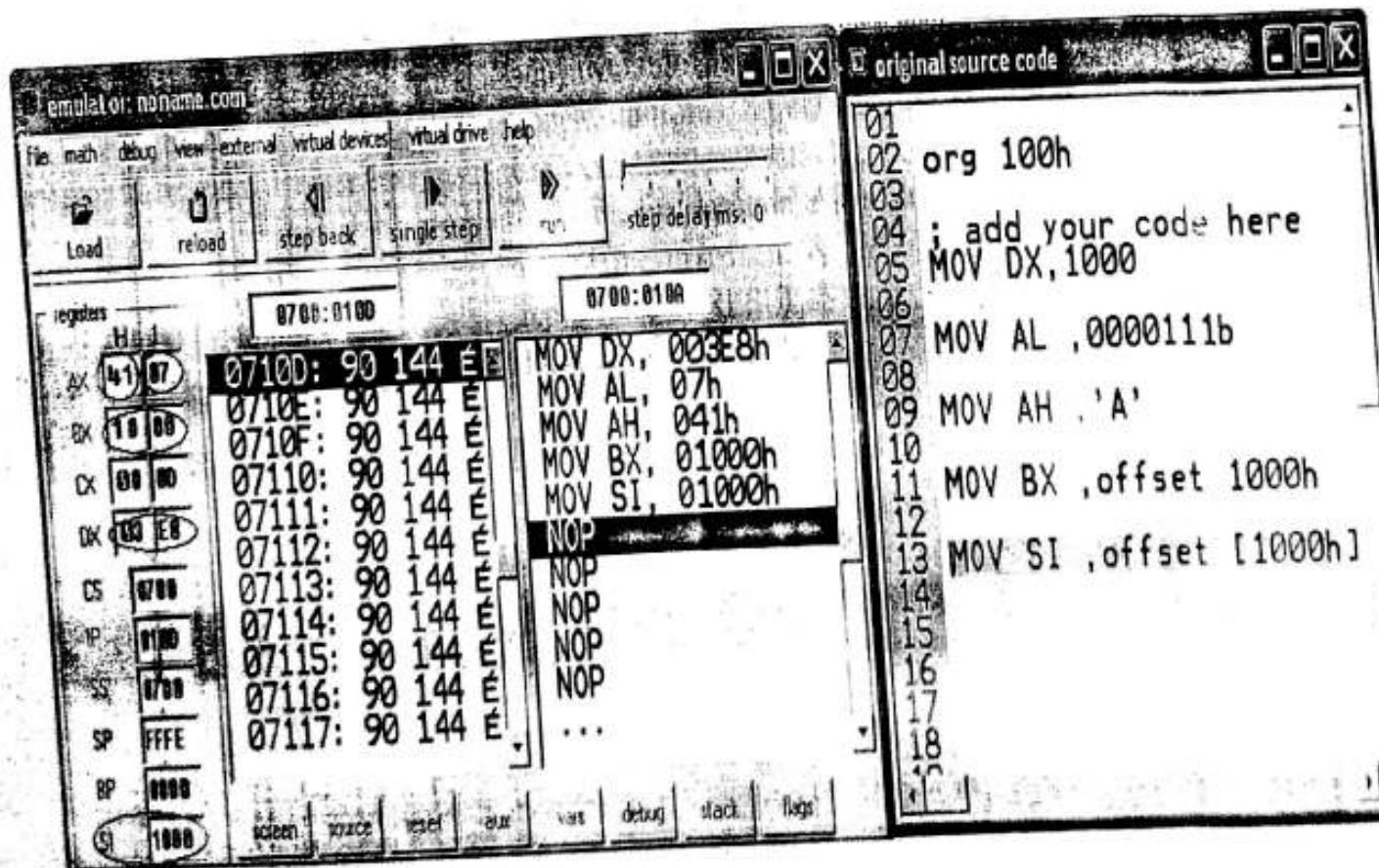
## EX

- MOV CX, 037AH
- MOV BL, [437AH]
- MOV AX, BX
- MOV DL, [BX]
- MOV DS, BX
- MOV RESULT [BP], AX

Put immediate number 037AH to CX  
Copy byte in DS at offset 437AH to BL  
Copy content of register BX to AX  
Copy byte from memory at [BX] to DL  
Copy word from BX to DS register  
Copy AX to two memory locations;  
AI to the first location, AH to the second;  
EA of the first memory location is sum of the displacement  
represented by RESULTS and content of BP.  
Physical address = EA + SS.

- MOV ES: RESULTS [BP], AX

Same as the above instruction, but physical address = EA + ES,  
because of the segment override prefix ES



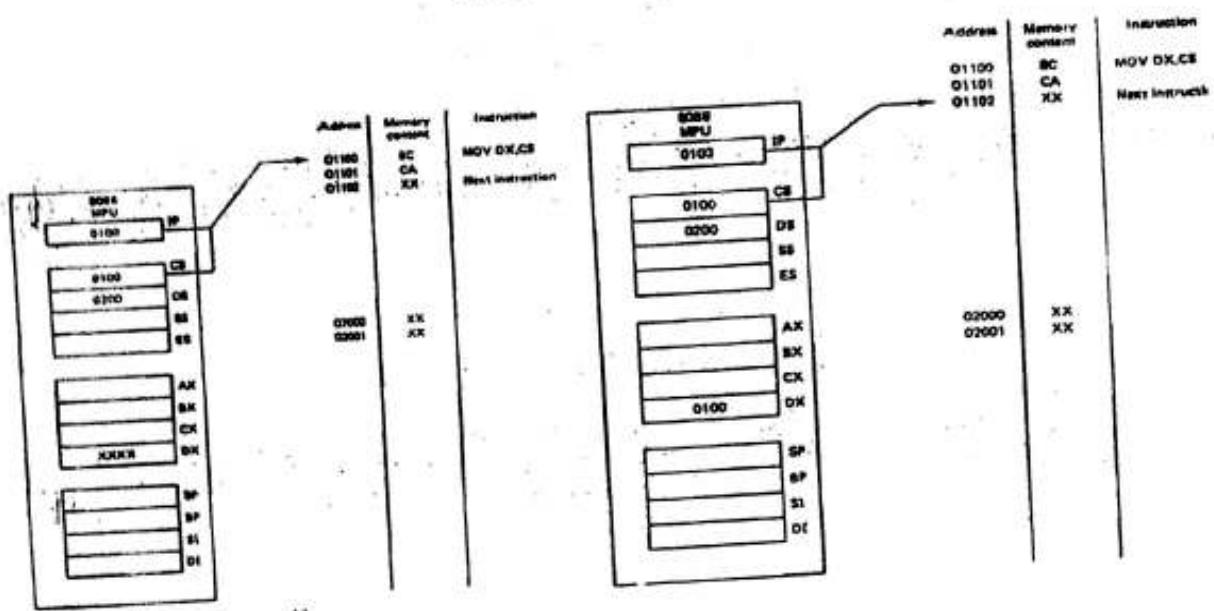
The image shows a debugger interface with two main windows. The left window is titled 'Registers' and shows the CPU register state at address 0700:0100. The right window is titled 'original source code' and displays assembly language code starting at address 01.

Registers	0700:0100	0700:0100
AX	41 00	0710D: 90 144 É
BX	10 00	0710E: 90 144 É
CX	00 00	0710F: 90 144 É
DX	00 1E	07110: 90 144 É
CS	0700	07111: 90 144 É
IP	0100	07112: 90 144 É
SS	1000	07113: 90 144 É
SP	FFFE	07114: 90 144 É
BP	0000	07115: 90 144 É
SI	1000	07116: 90 144 É
		07117: 90 144 É

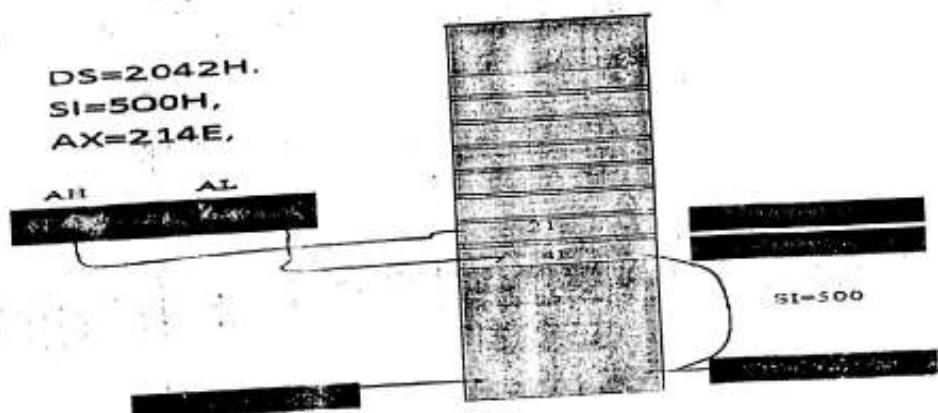
Original source code:

```
01
02 org 100h
03
04 ; add your code here
05 MOV DX, 1000
06
07 MOV AL, 0000111b
08
09 MOV AH, 'A'
10
11 MOV BX, offset 1000h
12
13 MOV SI, offset [1000h]
14
15
16
17
18
```

## MOV DX,CS



## MOV [SI],AX



### EXAMPLE

What is the effect of executing the instruction  
**MOV CX, [SOURCE\_MEM]**

Where **SOURCE\_MEM** equal to  $20_{16}$  is a memory location offset relative to the current data segment starting at  $1A000_{16}$ .

**Solution:**

$$((DS)0 + 20_{16}) \rightarrow (CL)$$

$$((DS)0 + 20_{16} + 1_{16}) \rightarrow (CH)$$

Therefore CL is loaded with the contents held at memory address

$$1A000_{16} + 20_{16} = 1A020_{16}$$

and CH is loaded with the contents of memory address

$$1A000_{16} + 20_{16} + 1_{16} = 1A021_{16}$$

### Notes:-

In order to say the compiler about data type, these prefixes should be used:  
**BYTE PTR** - for byte.  
**WORD PTR** - for word (two bytes).

For example

**MOV AL, byte PTR [SI]**

**MOV AX, WORD PTR [SI]**

Emu8086 supports shorter prefixes as well:

**b.** - for **BYTE PTR**

**w.** - for **WORD PTR**

**MOV AL ,b.[SI]**

**MOV AX ,W.[SI]**

### EX

Use the move instruction to copy the contents of memory offset 0300H to memory offset 0500H.

**MOV AL,[0300H]**

**MOV [0500H],AL**

### EX

Use the move instruction to copy the contents of memory offset 0300H and 0301H to memory offset 0500H and 0501H.

**MOV AX ,[0300H]**

**MOV [0500H] , AX**

**EX**

Write a program to store the data 15H , 75H into memory locations 0055H,01FCH. Assume DS=7000H.

```
MOV AX, 7000H  
MOV DS, AX  
MOV BX, 0055H  
MOV [BX], 15H  
MOV BX, 01FCH  
MOV [BX], 75H
```

**EX**

Write a program to **exchange** contents of memory location offset 3F00H with that of memory location offset FFC1H.

```
MOV AL,[3F00H]  
MOV BL,[FFC1H]  
MOV [3F00H],BL  
MOV [FFC1H],AL
```

## XC31G Exchange Instruction

- Can exchange A% with a 16 bit register.
- Can exchange an R bit register with another R bit register or with R bit register memory.
- Can exchange a 16 bit register with another 16 bit register or 16 bit memory.
- It cannot exchange two memory locations directly.

XC31G	Exchange	16bit	16bit	16bit
-------	----------	-------	-------	-------

XC31G Exchange	
Accumulator	Reg 16
Memory	Registers
Registers	Registers
Registers	Memory

Examples XC31G (1234H), B:

1001110000

101100

0111111000

XC31G A% B% A% \* → B%

XC31G AL,BH AL \* → BH

XC31G (BL,BH) (BL,BH) \* → BH

B%

For the data shown, what is the result of executing XC31G (BL,BH), B%?

BL=1234H, BH=1230H

Solutions:

6

100

Execution of this instruction performs the operation

$$((DS)0 + \text{SUM}) \leftrightarrow (\text{BX})$$

$$\text{PA} = 12000\text{H} + 1234\text{H} = 13234\text{H}$$

Then,

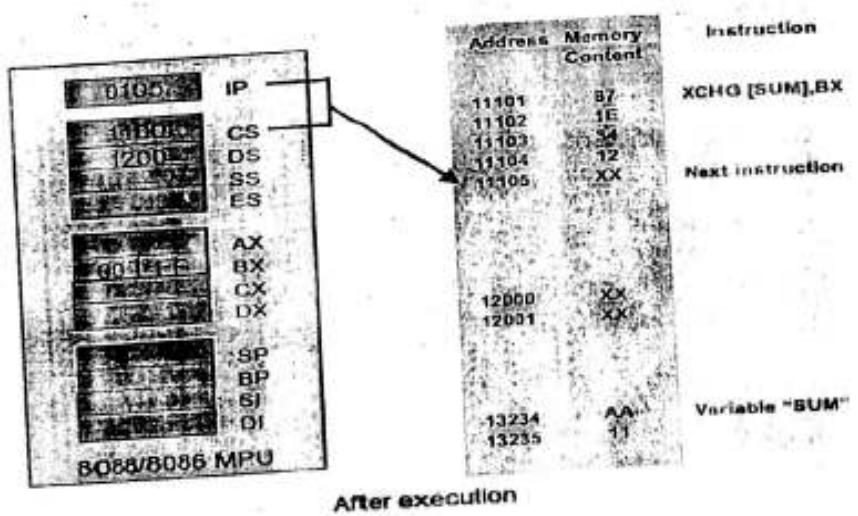
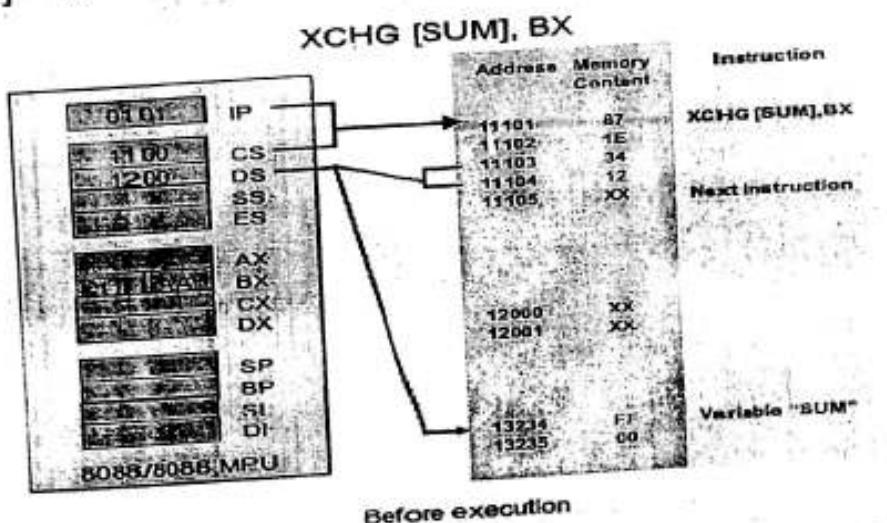
$$[13234\text{H}] \leftrightarrow (\text{BL})$$

$$[13235\text{H}] \leftrightarrow (\text{BH})$$

$$\text{Result: } (\text{BX}) = 00\text{FFH},$$

$$[13234] = \text{AA}$$

$$[13235] = 11$$



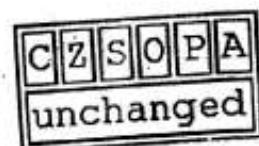
## Exchange Instruction

XCHG DX, [BX]

	Before	After
DX	1234H	
BX	1000H	
DS:1000H	ABCDH	
DS:1002H		1234H

Ex .

```
MOV AL, 5
MOV AH, 2
XCHG AL, AH ; AL = 2, AH = 5
XCHG AL, AH ; AL = 5, AH = 2
```



EX

```
MOV BX, 01FCH
MOV [BX], 50H
MOV AL, 90H
XCHG AL,[BX]
```

EX

```
MOV AX,5000H
MOV DS,AX
MOV BX,0100H
MOV [BX],0F1CH
MOV CX,5030H
XCHG CX,[BX]
```

## LEA, LDS, LES Instructions

The LEA, LDS, LES instructions provide the ability to manipulate memory references by translating either a 16-bit offset address into a general purpose register or a register together with a segment selector into either DS or ES.

Op	Op/Reg	Op/Reg	Op/Reg	Op/Reg
LEA	Load Effective Address	LEA Reg16,EA	EA... (Reg16)	None
LDS	Load Register And DS	DS Reg16,ES:EA	DS:MEM16... (Reg16) (Mem16*2) * (DS)	None
LES	Load ES, DS and DS	ES Reg16,ES:EA	ES:MEM16... (Reg16) (Mem16*2) * (ES)	None

### LEA Destination, Source

- Transfers the offset address of source (must be a memory location) to the destination register.

(REG = address of memory offset)

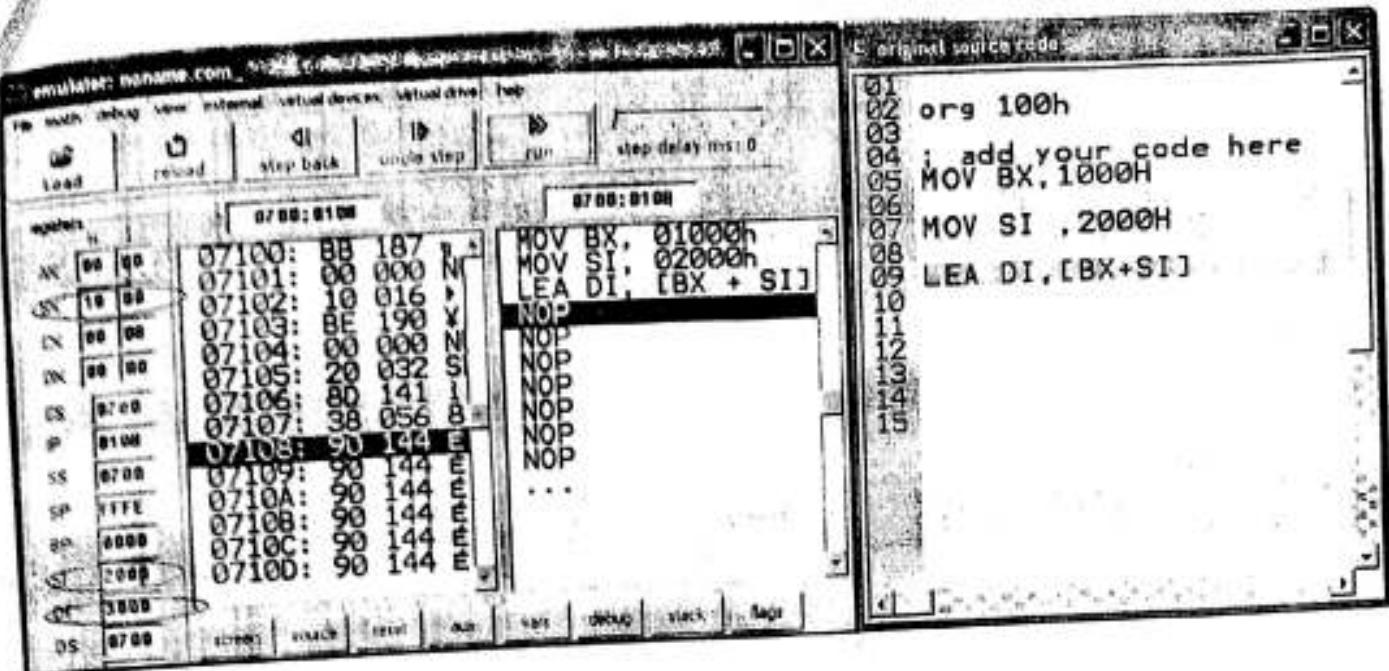
- It loads a 16-bit register with the offset address of the data specified by the source

Ex:

### LEA BX, [DI]

This instruction loads the contents of DI (offset) into the BX register.

- It does not modify flags.



LEA                    BX,NUMB

;NUMB is assumed to point at  
the byte at location 10FD in the  
data segment.

BL  $\leftarrow$  FD  
BH  $\leftarrow$  10

\* ~~LEA~~ LEA BX,NUMB = MOV BX,OFFSET NUMB

LEA            BX,[DI]

; BX  $\leftarrow$

DI

MOV            BX,[DI]

; BX  $\leftarrow$

[DI]

$\left\{ \begin{array}{l} \text{LEA } bx, si \\ \text{LEA } bx, [si] \\ \text{LEA } bx, offset\{si\} \\ \text{LEA } bx, offset si \end{array} \right.$

By comparing LEA with MOV, it's observed that:-

- LEA BX , [DI] load the offset address specified by [DI] (contents of DI) into BX register.

MOV BX , [DI] load the data stored at the memory location addressed by [DI] into register [DI].

## LDS Destination, Source

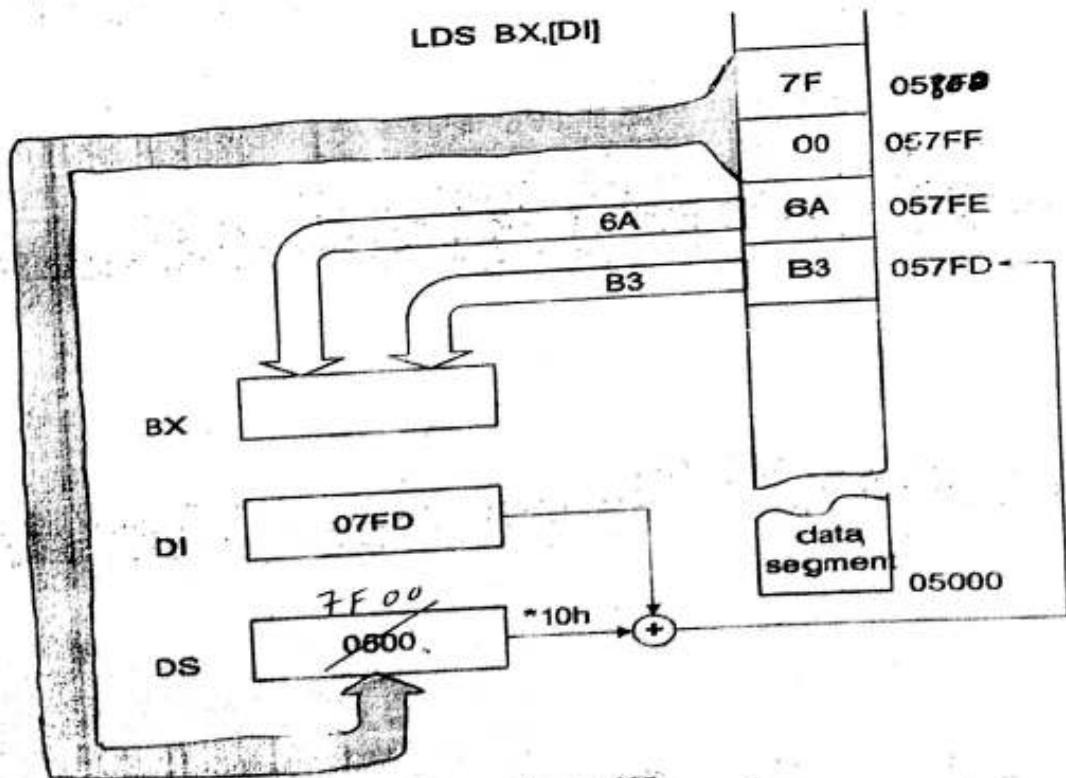
- Load 4-byte data (pointer) in memory to two 16-bit registers. It loads 32-bit pointer from memory source to destination register and DS.
- It does not modify flags
- The offset is placed in the destination register and the segment is placed in DS.
- Source operand gives the memory location.
- The first two bytes are copied to the register specified in the destination operand; the second two bytes are copied to register DS.

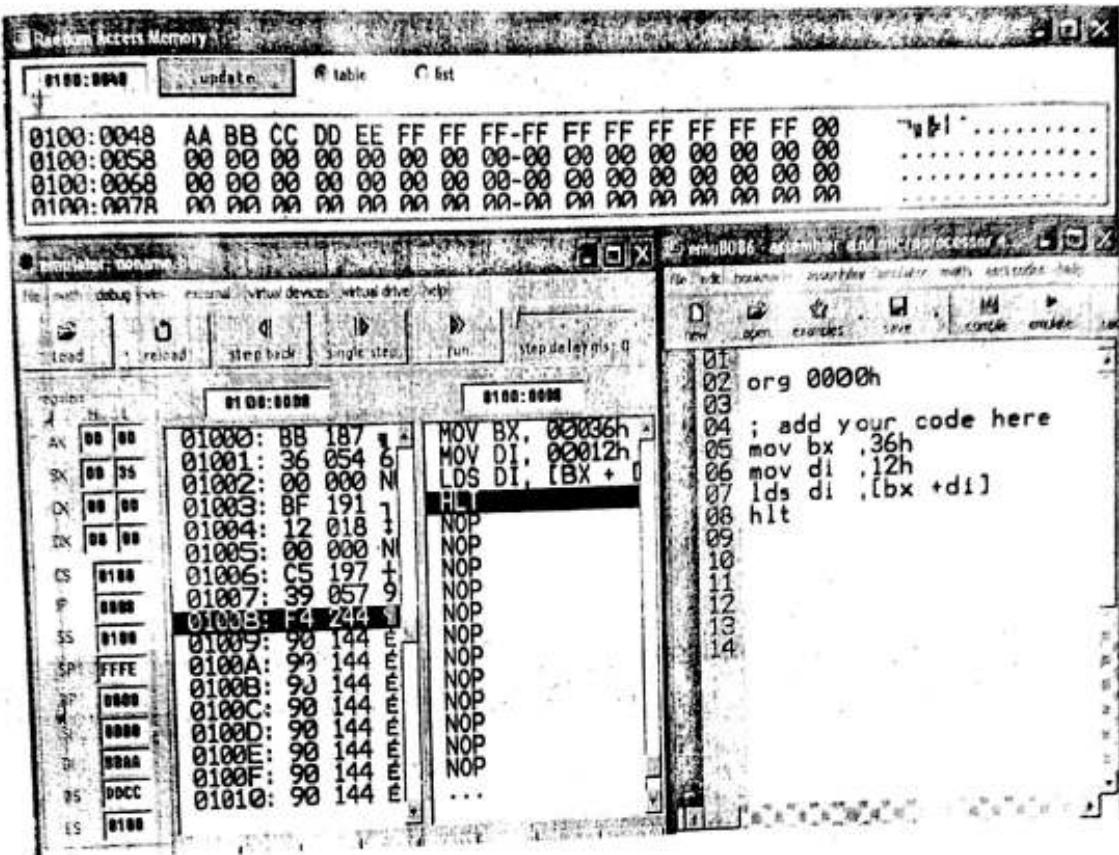
**REG = First word**

**DS = Second Word**

➤ LDS BX, [4326H]

Copy content of memory at displacement 4326H in DS to BL, content of 4327H to BH. Copy content at displacement of 4328H and 4329H in DS to DS register.





**Example:**

Assume DS = 500h, SI = 7D0h, BX = 2Dh,  
determine the contents of all the affected  
registers if the following instruction is  
executed:

LDS DI,[BX+SI]

23	057FF
4D	057FF
68	057FE
A2	057FD
data segment	
	05000

### LES Destination, Source

- It is identical to LDS except that the second two bytes are copied to ES.
- It does not modify flags.

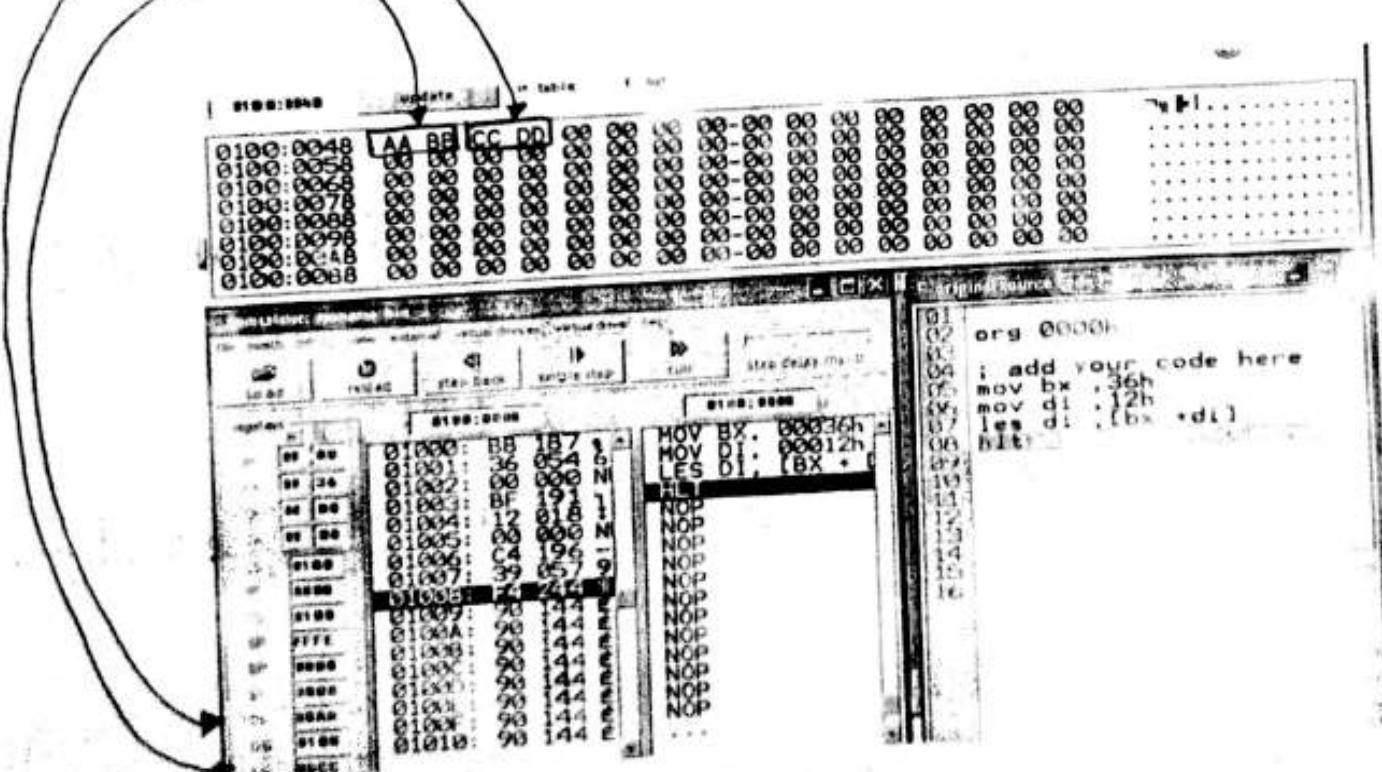
REG = first word  
ES = second word

→ LES BX, [789AH]

Copy content of memory at displacement 789AH in DS to BL,  
content of 789BH to BH, content of memory at displacement  
789CH and 789DH in DS is copied to ES register.

## ➤ LES DI, [BX]

Copy content of memory at offset [BX] and offset [BX] + 1 in DS to DI register. Copy content of memory at offset [BX] + 2 and [BX] + 3 to ES register.



2-Operand instruction to load ES and an Address Register from memory  
LES AR, M32

**LES DI,[3000H]**

Loads ES and DI using single instruction

Before  
ES 2000H After  
7000H

DI 1000H After  
6000H  
2000:3000H 6000H  
2000:3002H 7000H

2-Operand instruction to load an Effective address into an Address Register  
LEA AR, a16

EX

LEA BX, [SI]

Before  
BX 1000H After  
2000H

LEA BX, [SI] functionally same as

SI 2000H

MOV BX,SI

DS:2000H 3000H

2-Operand instruction to load DS and an Address Register from memory  
LDS AR, M32

EX

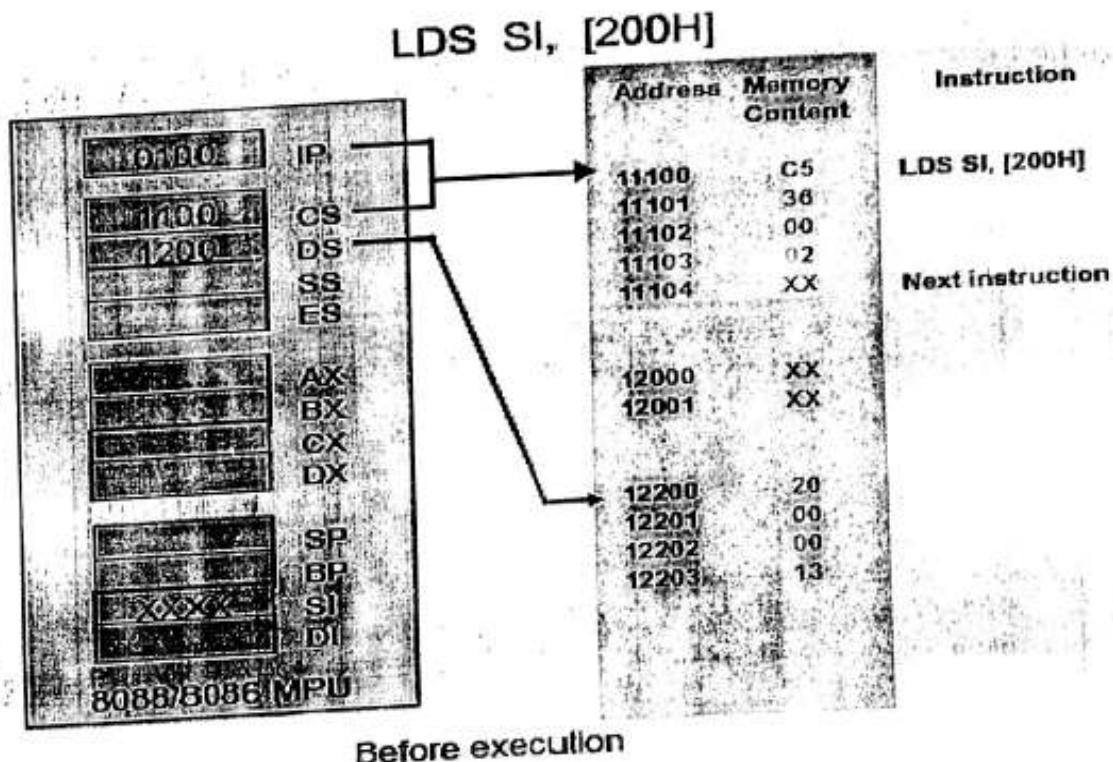
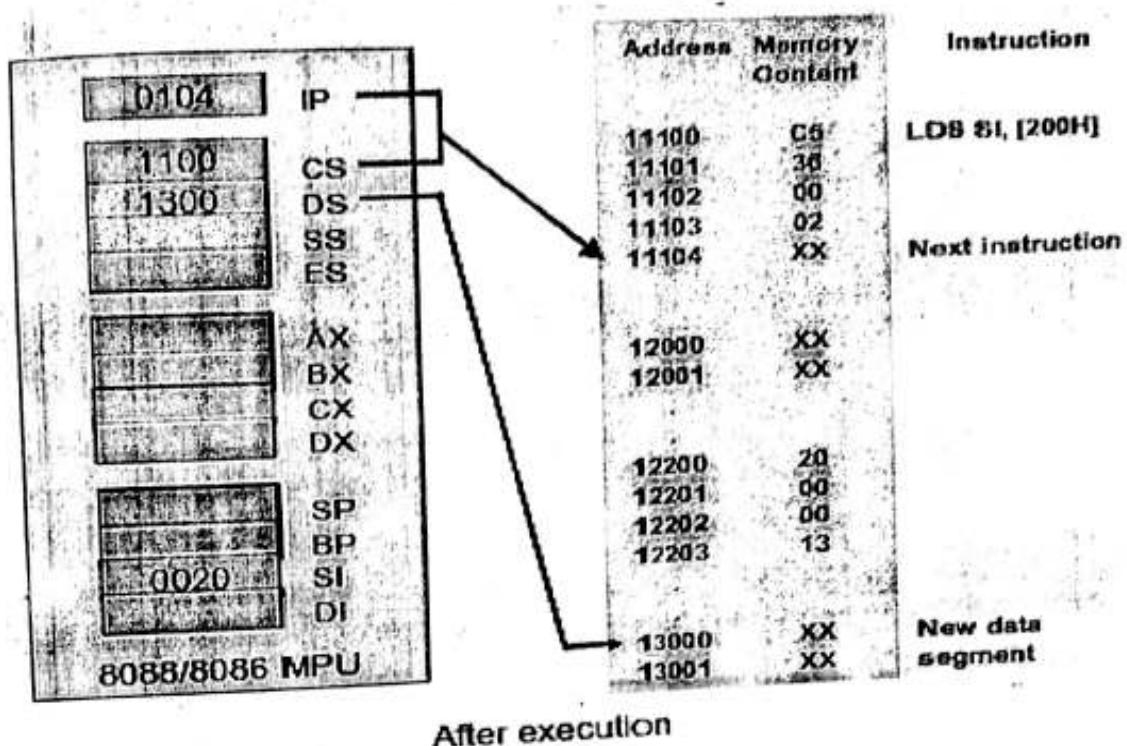
LDS SI,[3000H]

Loads DS and SI using single instruction

Before  
DS 2000H After  
7000H

SI 1000H

DS:3000H 6000H  
DS:3002H 7000H



Example 1 : Assuming that BX=20H ,DI=1000H , DS=1200H and the following memory contents:

Memory	12200	12201	12202	12203	12204
Content	11	AA	EE	FF	22

What result is produced in the destination operand by execution the following instruction?

a- LEA SI,[DI+BX+5]    b- LDS SI,[200]

Solution :

$$\begin{aligned} a- EA &= 1000 + 20 + 5 = 1025 \quad \text{then } (SI) = 1025 \\ b- PA &= DS:EA = DS * 10 + EA = 1200 * 10 + 200 = 12200 \\ &\therefore (SI) = AA11H \quad \text{and } (DS) = FFEEH \end{aligned}$$

### The LDS AND LES instructions

- LDS and LES load a 16-bit register with offset address retrieved from a memory location.
- then load either DS or ES with a segment address retrieved from memory.

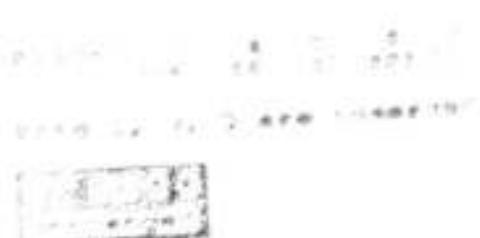
LDS	BL	BX,WORD PTR[SI];	
	BH	BX,WORD PTR[SI+1];	
	DS	BX,WORD PTR[SI+3:SI+2];	in the data segment
LES	BL	BX,WORD PTR[SI];	
	BH	BX,WORD PTR[SI+1];	
	ES	BX,WORD PTR[SI+3:SI+2];	in the extra segment

## LAHF

Copy AH to AH and the flags into AH

*It does not modify flags*

LAHF → AH ← Flags

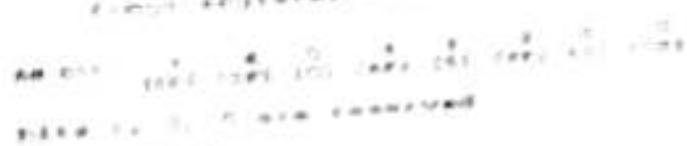


## SAHF

Move data in AH to AH and the flags into AH

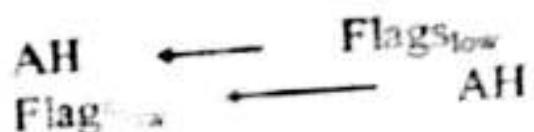
*It modifies flags: AF, CF, PF, SF, ZF*

SAHF → AH ← Flags



## The LAHF and SAHF instructions

LAHF  
SAHF



### EX

Write AH that save the contents of 80\*6's flag in memory location having an offset 1212 H and then to read the flags from the contents of the memory location having an offset 2121 H.

Load AH from flags

Move the contents of AH to memory location pointed to by offset 1212 H

Move the content of memory locations pointed to offset 2121H to AH

Store AH into flags

Stop

MOV AH, [2121]

SAHF  
HLT



## IN/OUT Instructions

- An **IN** instruction transfers data from an external I/O device to AL or AX.
- An **OUT** instruction transfers data from AL or AX to an external I/O device.
- The I/O device address is called port address.
- In direct addressing mode the address is a single byte.
- In indirect addressing mode the address is two bytes in DX.

IN AL,2EH ;AL ← port 2EH

IN AX,26H ;AL ← port 26H

                 ;AH ← port 27H

IN AL,DX ;AL ← port DX

IN AX,DX ;AL ← port DX

                 ;AH ← port DX+1

OUT 2EH,AL ; port 2EH ← AL

OUT 2EH,AX ; port 2EH ← AL

                 ; port 2FH ← AH

OUT DX,AL ; port DX ← AL

OUT DX,AX ; port DX ← AL

                 ; port DX+1 ← AH

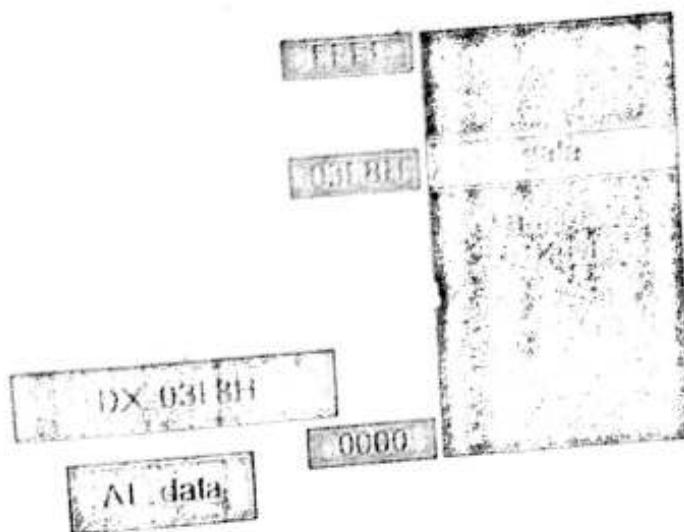
### Example

The serial port is at 03F8H(>255), read a byte from the serial port.

Since  $03F8H > 255$

```
MOV DX,03F8H
```

```
IN AL,DX
```



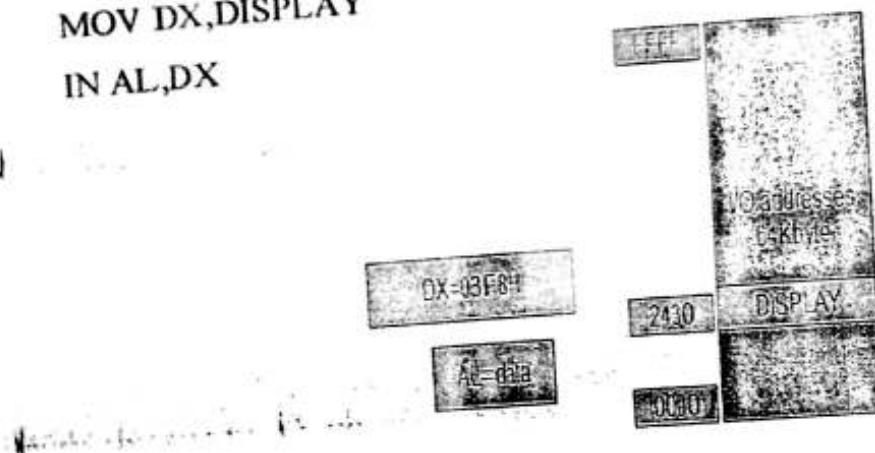
### Example

Define the DISPLAY device at 2430H and read a byte from it.

```
DISPLAY EQU 2430H
```

```
MOV DX,DISPLAY
```

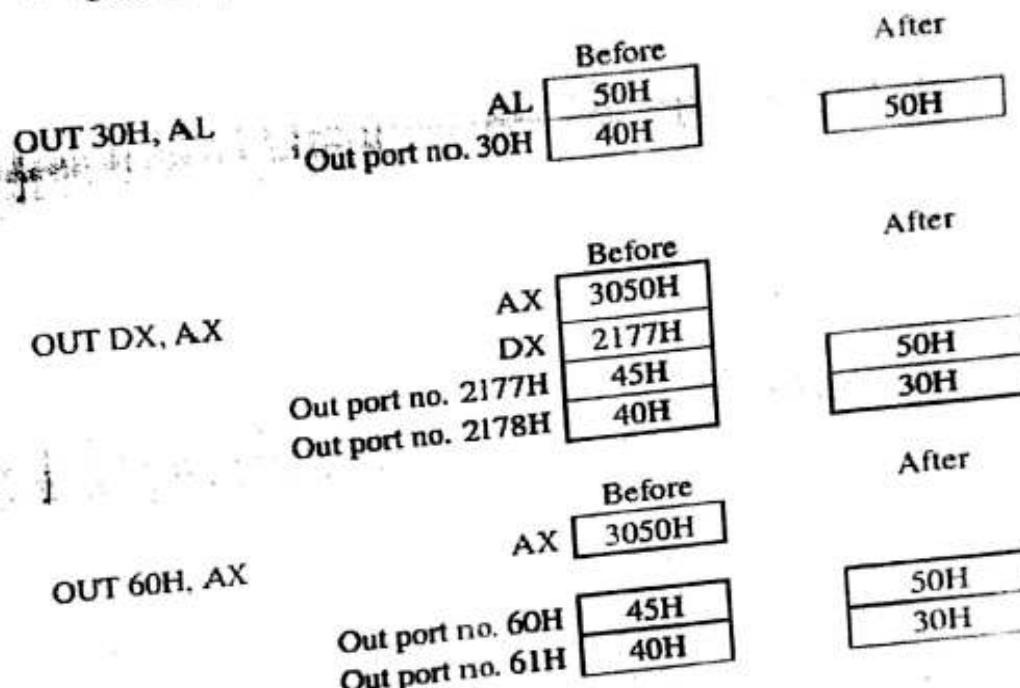
```
IN AL,DX
```



## OUT Instruction

### Syntax:

- OUT port address, AL ; can be AX or AL
- OUT DX, AL ; Just holds for DX



### Example:

Send char 'A' to the printer at 03A0H.

MOV DX,03A0H

MOV AL,'A'

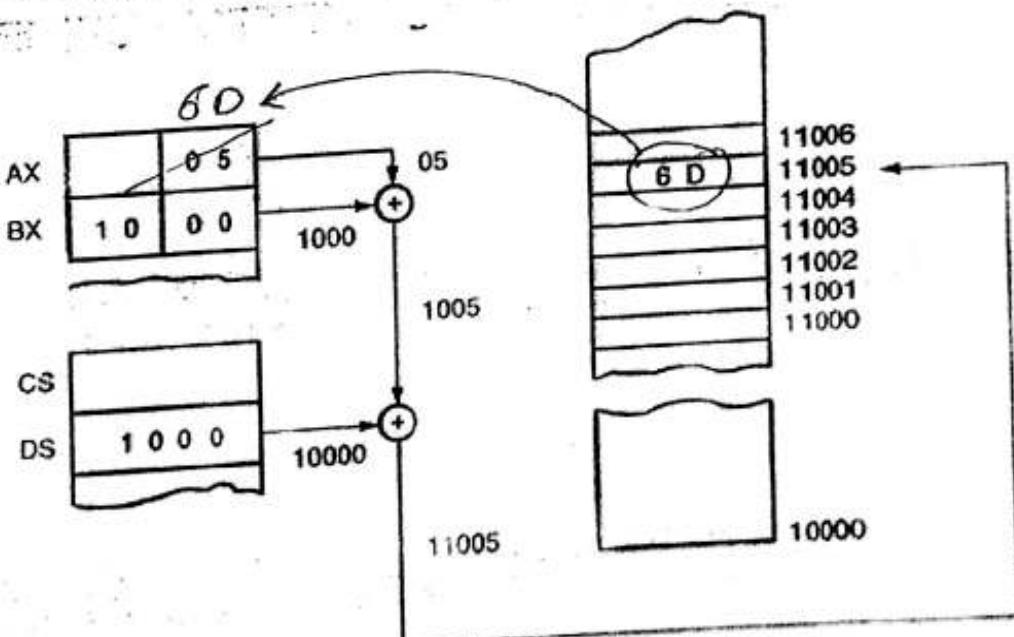
OUT DX,AL

## XLAT Instruction

**XLAT: Translate byte using look up table**

Mnemonic	Meaning	Format	Operation	Flags affected
XLAT	Translate	XLAT	$((AL)+(BX)+(DS)O) \rightarrow (AL)$	None

- Replace the data in AL with a data in a user defined **look-up table** (!!)
- BX stores the beginning address of the table.
- At the beginning of the execution, the number in AL is used as the index of the look-up table.
- It does not modify flags
- XLAT is the only instruction that adds 8 bit number to 16 bit number.
- XLAT called translate instruction, the operation of XLAT is changing the value of AL with the memory pointed to by (AL+BX).



### Example:

Assume (DS) = 0300H, (BX)=0100H, and (AL)=0DH

XLAT replaces contents of AL by contents of memory location with  
PA=(DS)0 +(BX) +(AL)

$$= 03000H + 0100H + 0DH = 0310DH$$

Thus

(0310DH)  $\rightarrow$  (AL)

- The translate (XLAT) data transfer instruction is shown below. It can be used for say an ASCII to EBCDIC code conversion.

- The content of BX represents the offset of the starting address of the look up table from the beginning of the current data segment while the content of AL represents the offset of the element which is to be accessed from the beginning of the look up table.

As an example, let DS = 0300 H, BX = 1234 H and AL = 05 H.

Hence, PA = 03000 H + 1234 H + 05 H = 04239 H

Thus, execution of XLAT would put the content of 04239 H into AL register. Conceptually, the content of 04239 H in EBCDIC should be the same as the ASCII character equivalent of 05 H.

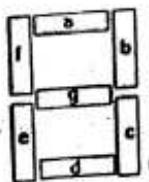
## EX

Suppose that a seven segment LED display lookup table is stored in memory at address TABLE, now XLAT can use this table to translate the BCD number in AL to a seven segment code also in AL.

Let TABLE = 1000H, DS=1000H,

a	b	c	d	e	f	g	
1	1	1	1	1	1	0	
0	1	1	0	0	0	0	
1	1	0	1	1	0	1	
1	1	1	1	0	0	1	
0	1	1	1	0	1	1	
1	0	1	1	0	1	1	
1	0	1	1	1	1	1	
1	1	1	0	0	0	0	
1	1	1	1	1	1	1	
1	1	1	1	0	1	1	

0	3FH
1	06H
2	5BH
3	4FH
4	66H
5	6DH
6	7DH
7	27H
8	7FH
9	6FH



The code for the operation of converting is very simple using XLAT

• TABLE DB 3FH,06H,5BH,4FH,66H,6DH,7DH,27H,7FH,6FH

• MOV AL,SOME\_BCD\_VALUE

• MOV BX,OFFSET TABLE

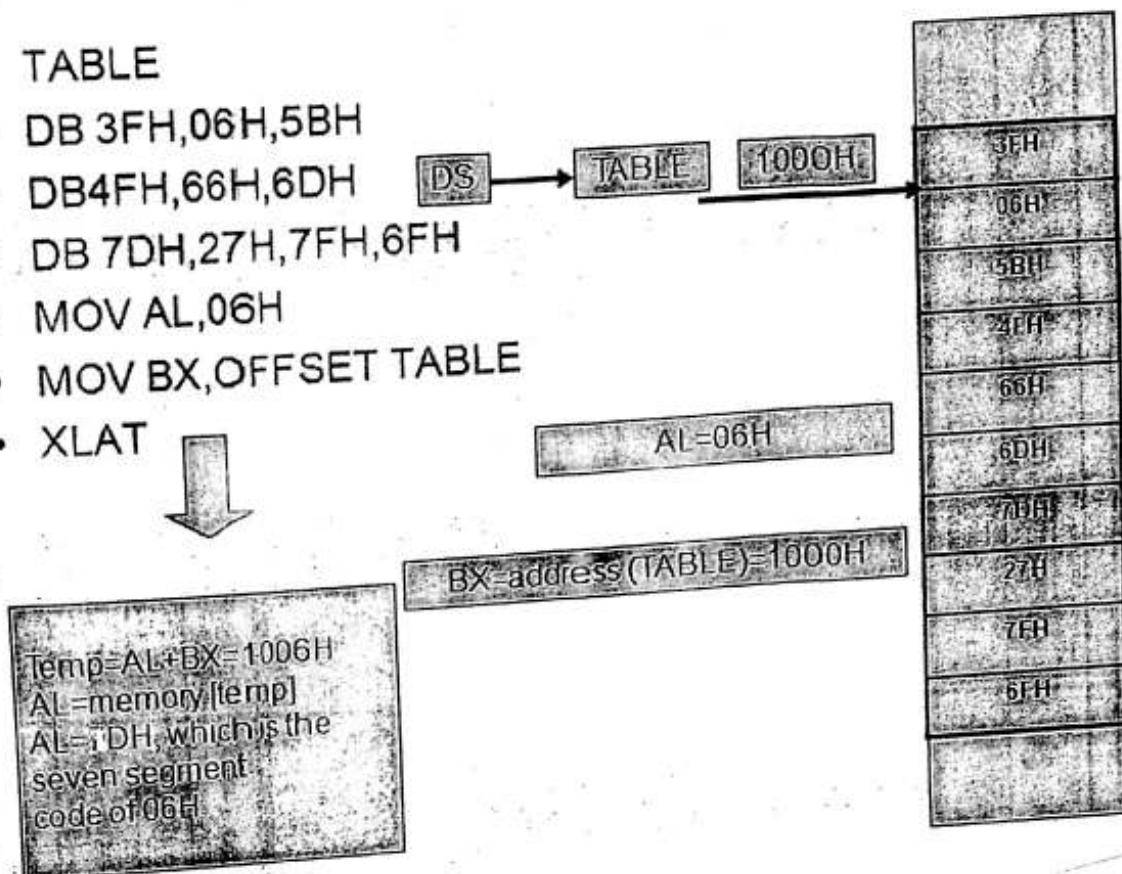
• XLAT

• For example take 06H(6 BCD) for the initial value of AL, after translation AL contains 7DH,

M [1] B [4] C [3]

7DH

- TABLE
- DB 3FH,06H,5BH
- DB4FH,66H,6DH
- DB 7DH,27H,7FH,6FH
- MOV AL,06H
- MOV BX,OFFSET TABLE
- XLAT



### EX

Write code to read the input key from port (60H) and output the value to a 7-segment display at 80H.

KEYS EQU 60H;

DISPLAY EQU 80H;

TABLE DB 3FH, 06H, 5BH, 4FH, 66H, 6DH, 7DH, 27H, 7FH, 6FH

LEA BX, TABLE;

IN AL, KEYS;

XLAT

OUT DISPLAY, AL

## PUSH and POP Instructions

The stack is used as temporary storage of registers and memory locations  
 PUSH is used to store data and POP is used to retrieve it back from the stack

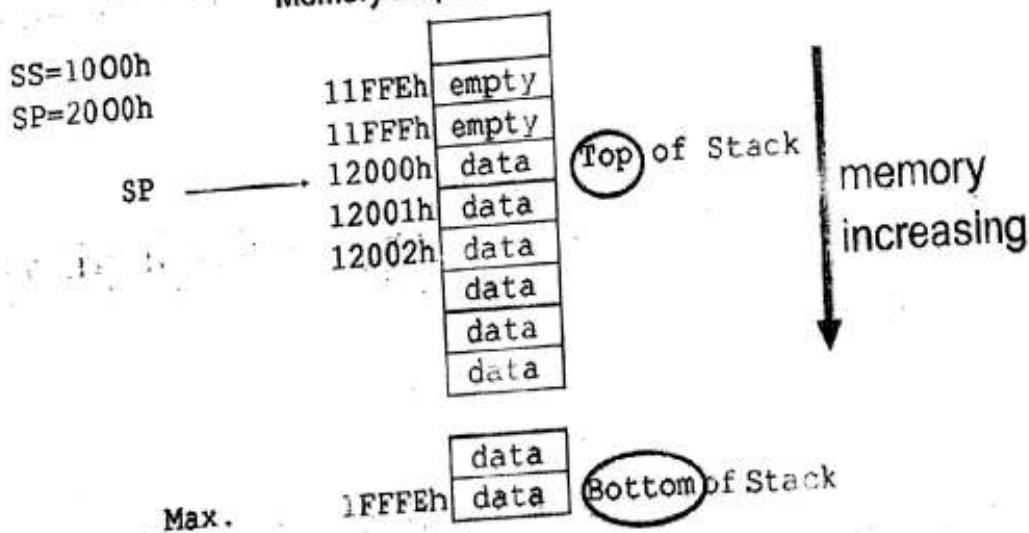
Mnemonic	Meaning	Format	Operation	Flags Affected
PUSH	Push word onto stack	PUSH S	$((SP)) \leftarrow (S)$ $(SP) \leftarrow (SP)-2$	None
POP	Pop word off stack	POP D	$(D) \leftarrow ((SP))$ $(SP) \leftarrow (SP)+2$	None

**Operand (S or D)**  
**Register**  
**Seg-reg (CS illegal)**  
**Memory**

- ⌘ The stack is a block of memory reserved for temporary storage of data and registers. Access is LAST-IN, FIRST-OUT (LIFO)
- ⌘ The last memory location used in the stack is given by (the effective address calculated from the SP register) and (the SS register):

### Example:

Memory Map of a stack



### **PUSH: Push to stack**

- It pushes the operand into top of stack.
- This instruction pushes the contents of the specified register/memory location on to the stack.
- The stack pointer is decremented by 2, after each execution of this instruction.

#### **Example**

PUSH AX

Decrement SP by 2 and copy AX to stack

PUSH DS

Decrement SP by 2 and copy DS to stack

PUSH [5000H]

Decrement SP by 2 and copy word from memory in DS

### **POP : Pop from stack**

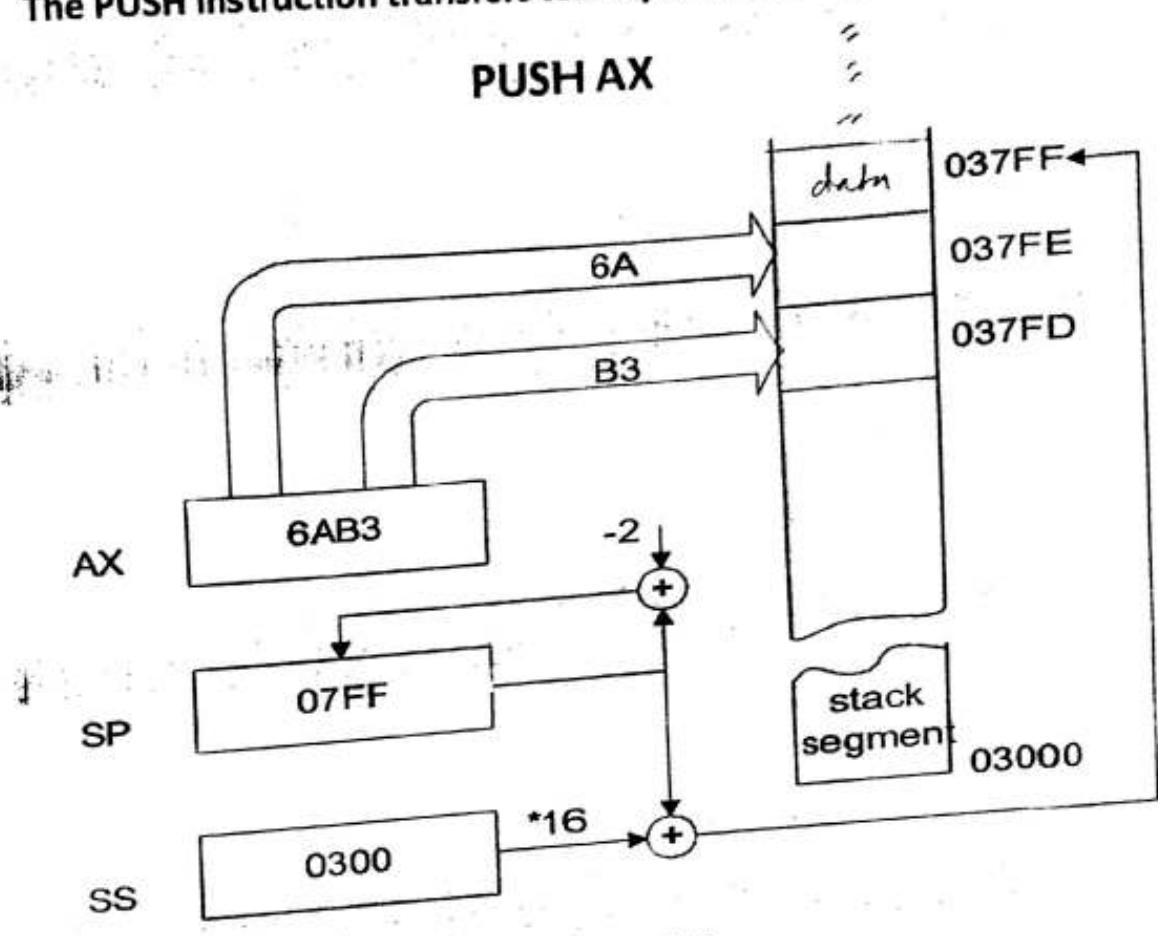
- It pops the operand from top of stack to Destination.
- The stack pointer is incremented by 2.
- Destination can be a general purpose register, segment register (except CS) or memory location.
- This instruction when executed, loads the specified register/memory location with the contents of the memory location of which the address is formed using the current stack segment and stack pointer.

POP AX

POP DS

POP [5000H]

The **PUSH** instruction transfers two bytes to the top of the stack.



**PUSH CX**

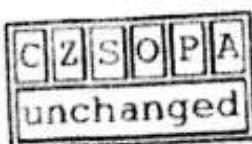
[SS:SP-1] ←	CH
[SS:SP-2] ←	CL
SP ←	SP-2

**PUSHF** (No operand)

The **PUSHF** (push flag) instruction copies the contents of the flag register to the stack.

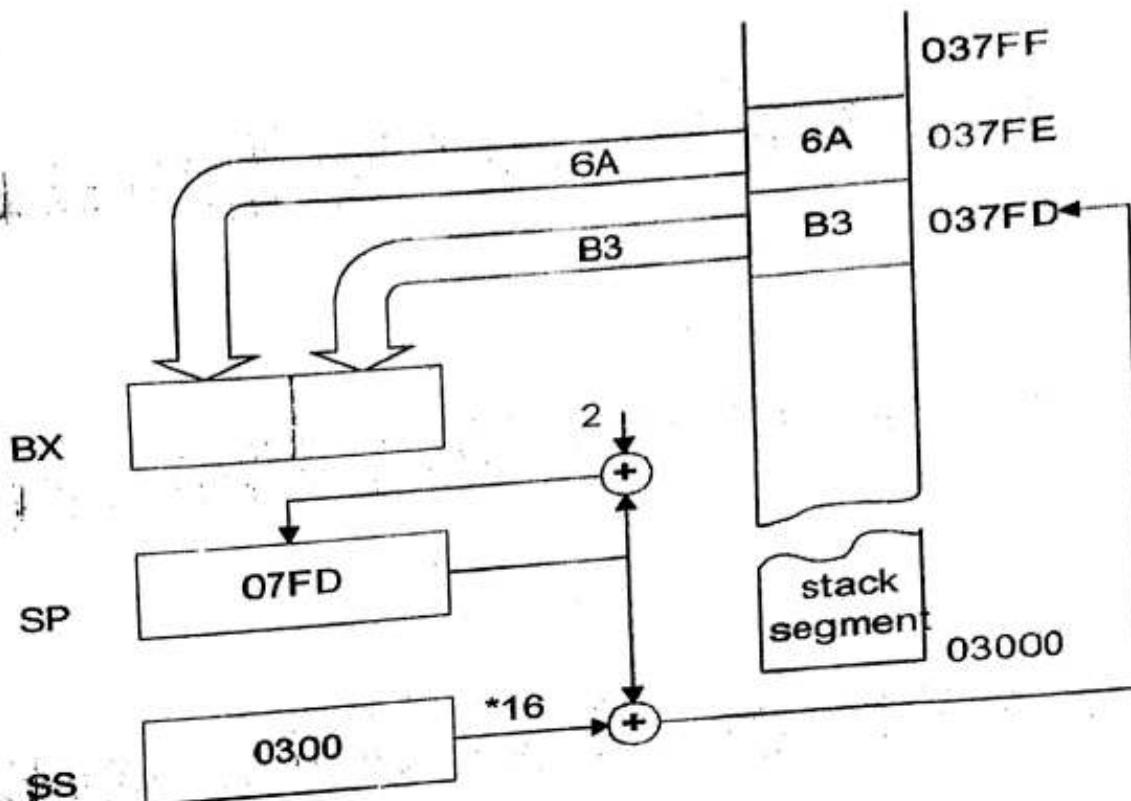
**Algorithm:**

SP = SP - 2  
SS:[SP] (top of the stack) = flags



The POP instruction performs the inverse operation of a PUSH instruction.

POP BX



## POP BX

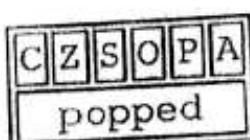
BL	←	[SS:SP]
BH	←	[SS:SP+1]
SP	←	SP+2

## POPF Algorithm:

(No operand)

Pops the stack top to flag register.

flags = SS:[SP] (top of the stack)  
SP = SP + 2



Ex:

Assuming that  $SP = 1236$ ,  $AX = 24B6$ ,  $DI = 85C2$ , and  $DX = 5F93$ , show the contents of the stack as each of the following instructions is executed:

PUSH AX

PUSH DI

PUSH DX

Solution:

SS:1230

SS:1231

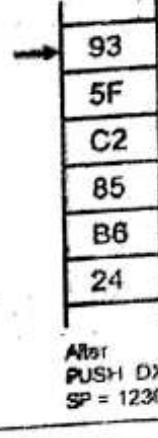
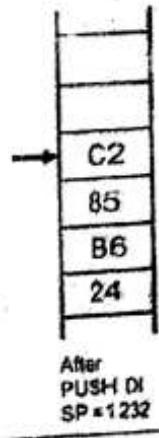
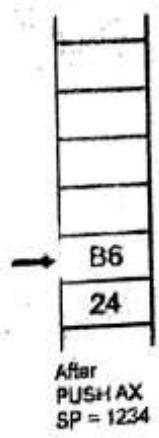
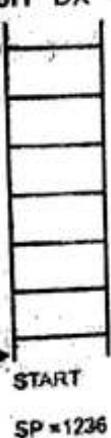
SS:1232

SS:1233

SS:1234

SS:1235

SS:1236



## Popping to stack

Ex:

Assuming that the stack is as shown below, and  $SP = 18FA$ , show the contents of the stack and registers as each of the following instructions is executed:

POP CX

POP DX

POP BX

Solution:

SS:18FA

SS:18FB

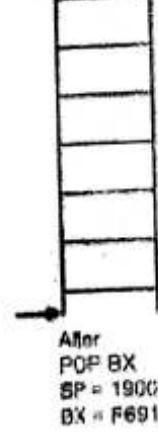
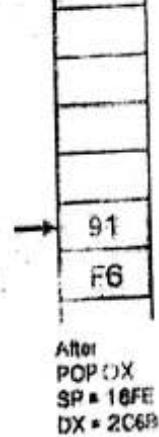
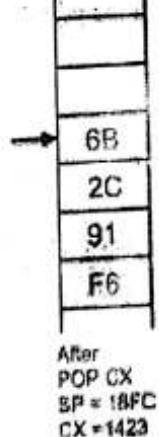
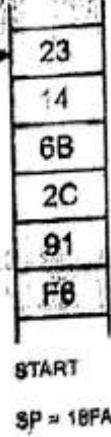
SS:18FC

SS:18FD

SS:18FE

SS:18FF

SS:1900



Ex Given SS=0105h , What is the outcome of the instruction

**PUSH AX**

BOS = 01050+FFFEh=1104h

SP=0008h

AX=1234h

TOS=01050+0008h=1058H

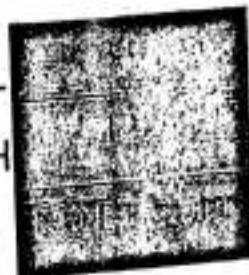
Decrement the SP by 2 and write AX into the word location 1056h

SS:0006 1056h AL

SS:0007 1057h AH

SS:0008 1058h

SP



Ex What is the outcome of the following instructions  
POP AX  
POP BX

If originally (SS:SP)=1056H

1056	34
1057	12
1058	BB
1059	AA

Read into the specified register from the stack and increment the stack pointer for each POP operation

At the first POP

At the second POP

(AX) = 1234h

(BX) = AABH and

(SS:SP) = 1058h

(SS:SP) = 105AH